REMARKS

Claims 1-20 are pending in the application and have been examined. Applicants acknowledge withdrawal of the anticipation rejection based on the Schilling reference. Applicants further acknowledge that applicants' admitted prior art is no longer used as a basis for the remaining obviousness rejection. The present office action is addressed as follows.

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bhat et al. (U.S. Patent No. 5,207,864) in view of Cohn et al. (U.S. Patent No. 7,276,789). Applicants traverse.

The examiner asserts that it would be obvious to combine Bhat and Cohn because Cohn discloses an alternative to the disclosed pressure application step in Bhat. Applicants respectfully disagree.

Bhat is directed to a process for fusing semiconductor wafers to one another, whereas Cohn concerns joining bonding features and target features together (See Bhat col. 4, lns. 57-64; Cohn col. 8, lns. 8-11, 34-40). Bhat discloses using heat and the application of pressure using a weight to bond semiconductor wafers. The thermocompressive process leads to a uniform fusion throughout the entire wafer hetero-interface, excepting small dislocations due to lattice mismatch (See Bhat, col. 4, lns. 15-20). That is, Bhat teaches that application of heat and pressure directly bonds the semiconductor wafers to one another, through chemical fusion, resulting in covalent bonding between wafers (See col. 4, lns. 57-64; col. 6, lns. 12-16).

In contrast, Cohn teaches that raised bonding features 160 and complementary target features 160' are formed on the surface of the substrates (See Cohn, col. 7, lns. 29-34; col. 8, lns. 1-4). The bonding features 160 and target features 160' assume shapes such as bumps, lines, and rings, and are formed from a bonding material deposited on the substrate surface (col. 7, lns. 34-37). For example, the features can be formed from using an electroplating process in which titanium-tungsten is sputter deposited on the substrate surface, sputter depositing gold on top of the titanium-tungsten, and electroplating gold on top of the sputter-deposited gold so that the bonding features reach a height of at least 3 microns (See col. 7, lns. 48-56). Target features 160' are formed using a similar process, but have a height of 0.1-1.0 microns (col. 8, lns. 11-15). During thermocompression bonding of the substrates, the bonding features and target features plastically deform so that they are compressed to approximately 50% of their original height (col. 8, lns. 34-40). That is, a gap of 1.55 to 2 microns remains between the substrates. Thus, while the substrates are bonded through bonding material, they are not chemically fused, as disclosed in Bhat. Put another way, the process described by Cohn does not fuse the substrates as disclosed in Bhat. Instead, the process merely fuses metal bonding features. Since Cohn fails to disclose chemical fusion of the substrates, applicants assert that there one of skill in the art would not modify the wafer fusion process disclosed by Bhat using the bonding process disclosed by Cohn.

Further, the examiner asserts that an artisan would have been motivated to find a way to create stronger and/or more efficient bonds when using the wafer fusion

method disclosed in Bhat. However, while Bhat is directed to semiconductor wafer fusion, Cohn fails to disclose any such fusion of semiconductor substrates. Instead Cohn merely discloses the bonding of substrates using a metallic bonding and target features (Cohn, col. 7, lns. 48-56; col. 8, lns. 11-15). Additionally, while isostatic pressing may adequately bond metals as described in Cohn, Bhat teaches that uniaxial pressure provided by a weight is necessary for bonding semiconductor wafers (Bhat col. 3, lns. 43-46). Accordingly, an artisan would not consider the isostatic pressing in Cohn to be the equivalent of the uniaxial pressing described in Bhat. For these reasons, applicants respectfully request withdrawal of the rejection of claim 1-20.

Moreover, even assuming, *arguendo*, that one of skill in the art would modify the process disclosed by Bhat based on the process of Cohn, the resulting modified process still fails to disclose the features of the present invention. As discussed previously, Bhat teaches that a molybdenum weight is placed on top of the pair of wafers to ensure close contact between wafers (See col. 3, lns. 43-45). The reference teaches that a weight is necessary to maintain the physical proximity of the wafers (See Bhat, col. 2 line 68 – col. 3, line 1). That is, Bhat appears to teach that a weight is necessary to create a bond between the wafers. The general assumption in the art at the time of this invention was that a step of isostatic pressing following the step of bringing, without some protection of the wafers to be bonded, would break the weak bond formed between the wafers (see applicants' Specification p. 10, lns. 1-5; p. 5, ln. 26 - p. 6, ln. 5).

Similarly, while Cohn discloses that hot isostatic pressing can be used to bond semiconductor substrates, the reference teaches that the substrate pair must be placed into a high-temperature bag made from polyimide or metal foil, and subject the entire bag to hot-isostatic-pressing (See Cohn, col. 10, lns. 9-12). That is, Cohn teaches that protection of the substrate pair is required during hot isostatic pressing to prevent the wafers from splitting apart. Specifically, Cohn relies on encapsulating the substrates in a high-temperature bag to prevent separation of the substrates.

In contrast, claims 1 and 19 of the present application recite that a step of bringing forms a weak bond between the wafers, and that steps of applying bonding pressure and heat are performed after the step of bringing. This order allows for application of heat and pressure to the weakly bonded wafers without the need for a weight, and without encapsulating the wafers prior to heating and applying pressure thereto (See Applicants' Specification, p. 5, lns. 26-30; p. 9, lns. 23-26). The weak bond between wafers prevents gas or liquid from penetrating the interface between the two wafers, and the pressure acts on the exposed surfaces of the wafer pair to form a strong bond (p. 5, lns. 26-28). Moreover, the lack of a weight or encapsulation eliminates unnecessary steps in production of bonded wafers and allows for application of heat and pressure to multiple pairs of wafers simultaneously, advantageously increasing the speed and efficiency of the process disclosed in the present application (p. 5, ln. 30 – p. 6, ln. 5). Since Bhat and Cohn, taken alone or in combination, fail to disclose steps of applying heat and bonding pressure following a step of bringing as recited in independent

claims 1 and 19, applicants again request withdrawal of the rejection of claims 1 and 19, and their respective dependent claims.

Regarding claim 4, the examiner asserts that Bhat discloses a process for improving bonding, which implicitly means strengthening bonding. Bhat is directed to a method for low-temperature fusion of dissimilar semiconductors. However, Bhat fails to disclose a feature of creating a temperature or pressure ramp. Instead, the reference merely teaches that a 200 g weight is placed on a pair of semiconductor wafers to be joined, and that the graphite susceptor is used to heat the wafers to a temperature of 650° C (See Bhat, col. 3, lns. 43-50). In contrast, Figs. 1A and 1B of the present specification show temperature and pressure ramps that indicate at least the relative starting times and durations of the applied temperature and pressure, as well as the rate of increase in temperature and pressure. Since Bhat fails to disclose creation temperature and pressure ramps as recited in claim 4, applicants again request withdrawal of the rejection of claim 4 and its dependent claim 5.

Moreover, with respect to claim 5, since Bhat fails to disclose creation of temperature and pressure ramps, it necessarily follows that Bhat also fails to disclose creation of a temperature ramp that is independent of the pressure ramp. For this additional reason, applicants again request withdrawal of the rejection of claim 5

Regarding claim 6, the examiner asserts that Bhat discloses that a step of heating commences prior to a step of applying pressure. However, the Abstract of Bhat teaches that "while the wafers are forced together under moderate pressure...the

temperature is raised to 650° C" (See Abstract, lns. 6-8). This implies that the wafers are under pressure prior to raising the temperature. Since Bhat fails to disclose a step of heating that begins before a step of applying pressure, applicants again request that the rejection of claim 6 be withdrawn.

Regarding claim 13, the examiner asserts that a choice between direct bonding (i.e., bonding surfaces in direct contact with one another, without an intervening layer) and indirect bonding (i.e., bonding surfaces with an interlayer between the surfaces) is a matter of design choice, and that one of ordinary skill in the art would choose between these bonding types based on the teachings of Bhat and Cohn. However, Bhat discloses that residual acid remaining between semiconductor wafers is removed using a spin drier prior to application of pressure and heat (See Bhat, col. 5, ln. 67 – col. 6, ln. 2). Moreover, Bhat teaches that pressure is applied so that the wafers are held in physical proximity during the bonding process (See col. 2, ln. 64 – col. 3, ln. 1). This implies that the semiconductor wafers must be in direct contact for bonding to take place. Accordingly, one of ordinary skill in the art would not have been motivated to use the wafer fusion method disclosed in Bhat for indirect wafer bonding. Moreover, use of an interlayer is more than a simple design choice, as the presence or absence of an interlayer can result in different physical properties of the bonded semiconductors. For these reasons, applicants again request withdrawal of the rejection of claim 13.

With respect to claim 17, the examiner asserts that Bhat discloses carrying out the steps of applying, heating, and controlling and maintaining with a plurality of

pairs of wafers simultaneously. However, this is not the case. While Bhat does refer to plural wafers, the reference is silent regarding plural pairs of wafers. Moreover, Bhat discloses that if one of the wafers is silicon, the pair of wafers is assembled in hydrofluoric acid, and then the assembly is placed in a furnace for annealing (See Bhat, Abstract). Applicants note that Bhat references only a single assembly (See Bhat, Abstract; col. 3, lns. 50-52; col. 6, lns. 3-5). For this reason, applicants again request withdrawal of the rejection of claim 17.

Regarding claim 20, applicants additionally traverse this rejection because the cited references fail to disclose or suggest inducing strain in a semiconductor wafer as part of the bonding process. The examiner asserts that strain is an inherent product of the heat and pressure used in the bonding process. Applicants disagree. Neither Bhat nor Cohn discloses subjecting the substrates to be bonded to any specific strain. Instead, the references merely teach that compressive force is used to bond substrates. In contrast, the present specification teaches that strains in the bonded wafers can be tailored by changing a level of pressure (See applicants' Specification, p. 6, lns. 26-27). Because the references are silent regarding inducing a strain in one or more of the substrates, as recited in claim 20, applicants again request withdrawal of the rejection of claim 20.

For all of the foregoing reasons, applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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